Pin Name (1)	**208-Pin PQFP**	**256-Pin FineLine BGA**	**484-Pin FineLine BGA**
MSEL0 (2)	108	P1	U4
MSEL1 (2)	107	R1	V4
nSTATUS(2)	52	T16	W19
nCONFIG (2)	105	N4	T7
DCLK (2)	155	B2	E5
CONF_DONE (2)	2	C15	F18
INIT_DONE (3)	19	G16	K19
nCE (2)	154	B1	E4
nCEO (2)	3	B16	E19
nWS (4)	206	B14	E17
nRS (4)	204	C14	F17
nCS (4)	208	A16	D19
CS (4)	207	A15	D18
RDYnBSY (4)	16	G14	K17
CLKUSR (4)	10	D15	G18
DATA7 (4)	166	B5	E8
DATA6 (4)	164	D4	G7
DATA5 (4)	162	A4	D7
DATA4 (4)	161	B4	E7
DATA3 (4)	159	C3	F6
DATA2 (4)	158	A2	D5
DATA1 (4)	157	B3	E6
DATA0 (2), (5)	156	A1	D4
TDI (2)	153	C2	F5
TDO (2)	4	C16	F19
TCK (2)	1	B15	E18
TMS (2)	50	P15	U18
TRST (2)	51	R16	V19
Dedicated Inputs	78, 80, 182, 184	B9, E8, M9, R8	E12, H11, R12, V11
Dedicated Clock Pins	79, 183	A9, L8	D12, P11
GCLK1 (6)	79	L8	P11
LOCK (7)	62	P12	U15
DEV_CLRn (3)	180	D8	G11
DEV_OE (3)	186	C9	F12
VCCINT (2.5 V)	21, 33, 48, 72, 91, 106, 124, 130, 152, 185, 201	E11, F5, F7, F9, F12, H6, H7, H10, J7, J10, J11, K9, L5, L7, L12, M11, R2	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P15, R14, V5, W21, Y8, AA12
VCCIO (2.5 or 3.3 V)	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	D12, E6, F8, F10, G6, G8, G11, H11, J6, K6, K8, K11, L10, M6, N12	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13
VCC_CKLK (8)	77	L9	P12

Pin Name (1)	**208-Pin PQFP**	**256-Pin FineLine BGA**	**484-Pin FineLine BGA**
GND	6, 20, 23, 32, 35, 43, 49, 59, 76, 82, 109. 117, 123, 129, 137, 145, 151, 171, 181, 188	A3, A14, C7, E5, E12, F6, F11, G7, G9, G10, H8, H9, J8, J9, K5, K7, K10, L1, L6, L11, M5, M12	A1, A8, A22, B1, B2, B17, B21, B22, C2, C21, D6, D17, E21, F10, G3, G21, H2, H8, H15, J9, J14, J20, K3, K10, K12, K13, L11, L12, M11, M12, M20, N8, N10, N13, P4, P9, P14, R8, R15, R22, T1, V3, W20, Y1, Y2, Y3, Y21, Y22, AA1, AA6, AA22, AB11, AB16
GND_CKLK (8)	81	T8	W11
No Connect (N.C.)	–	–	A2, A3, A4, A5, B3, B4, B10, C17, F2, J2, K2, L2, N1, P20, P22, R3, T20, T21, U1, W22, Y16, AA15, AB3, AB4, AB5, AB7, AB15, AB17, AB18, AB19, AB20
Total User I/O Pins (9)	147	186	333

Notes:

(1) All pins that are not listed are user I/O pins.

(2) This pin is a dedicated pin; it is not available as a user I/O pin.

(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(4) This pin can be used as a user I/O pin after configuration.

(5) This pin is tri-stated in user mode.

(6) This pin drives the ClockLock and ClockBoost circuitry.

(7) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK goes low if a periodic clock stops clocking. The LOCK pin is optional; if the LOCK output is not used, this pin is a user I/O pin.

(8) This pin is the power or ground for the ClockLock and ClockBoost circuitry of a PLL. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. If the PLL is not used, this power or ground pin should bew connected to VCCINT or GNDINT, respectively.

(9) The user I/O pin count includes dedicated inputs, dedicated clock inputs, and all I/O pins.