FEATURES

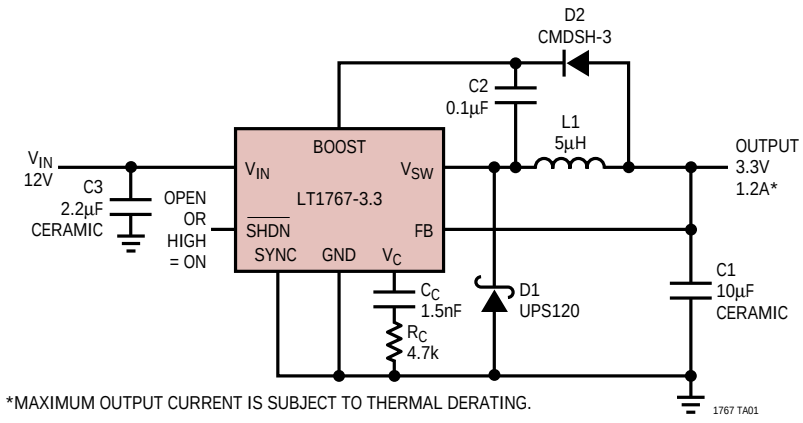
DESCRIPTION

APPLICATIONS

- Portable Computers
- Wall Adapters
- Battery-Powered Systems
- Distributed Power

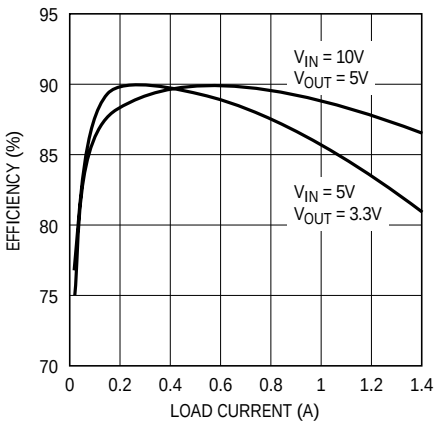
TYPICAL APPLICATION

12V to 3.3V Step-Down Converter



*MAXIMUM OUTPUT CURRENT IS SUBJECT TO THERMAL DERATING.

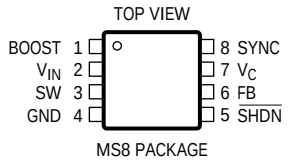
Efficiency vs Load Current



ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage 25V
BOOST Pin Above SW 20V
Max BOOST Pin Voltage 35V
SHDN Pin 25V
FB Pin Voltage 6V
FB Pin Current 1mA
SYNC Pin Current 1mA
Operating Junction Temperature Range (Note 2)
LT1767E ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

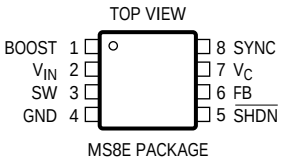


MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

GROUND PIN CONNECTED
TO LARGE COPPER AREA

ORDER PART NUMBER
LT1767EMS8
LT1767EMS8-1.8
LT1767EMS8-2.5
LT1767EMS8-3.3
LT1767EMS8-5
MS8 PART MARKING
LTLS
LTWG
LTWD
LTWE
LTWF



MS8E PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 40°C/W

EXPOSED GND PAD
CONNECTED TO LARGE
COPPER AREA ON PCB

ORDER PART NUMBER
LT1767EMS8E
LT1767EMS8E-1.8
LT1767EMS8E-2.5
LT1767EMS8E-3.3
LT1767EMS8E-5
MS8E PART MARKING
LTZG
LTZH
LTZJ
LTZK
LTZL

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, V_C = 0.8V, Boost = V_{IN} + 5V, SHDN, SYNC and switch open unless otherwise noted.

PARAMETER	CONDITION			MIN	TYP	MAX	UNITS
Maximum Switch Current Limit	T_A = 0°C to 125°C T_A = –40°C			1.5 1.3	2	3 3	A A
Oscillator Frequency	3.3V ≤ V_{IN} ≤ 25V		 ●	1.1 1.1	1.25	1.4 1.5	MHz MHz
Switch On Voltage Drop	I_{SW} = –1.5A, 0°C ≤ T_A ≤ 125°C and –1.3A, T_A < 0°C		 ●		330	400 500	mV mV
V_{IN} Undervoltage Lockout	(Note 3)		●	2.47	2.6	2.73	V
V_{IN} Supply Current	V_{FB} = V_{NOM} + 17%		●		1	1.3	mA
Shutdown Supply Current	$\overline{SHDN}$ = 0V, V_{IN} = 25V, V_{SW} = 0V		 ●		6	20 45	µA µA
Feedback Voltage	3V ≤ V_{IN} ≤ 25V, 0.4V < V_C < 0.9V (Note 3)	LT1767 (Adj)	 ●	1.182 1.176	1.2	1.218 1.224	V V
		LT1767-1.8	●	1.764	1.8	1.836	V
		LT1767-2.5	●	2.45	2.5	2.55	V
		LT1767-3.3	●	3.234	3.3	3.366	V
		LT1767-5	●	4.9	5	5.1	V
FB Input Current	LT1767 (Adj)		●		–0.25	–0.5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, V_C = 0.8V, Boost = V_{IN} + 5V, $\overline{SHDN}$, SYNC and switch open unless otherwise noted.

PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
FB Input Resistance	LT1767-1.8	●	10.5	15	21	kΩ
	LT1767-2.5	●	14.7	21	30	kΩ
	LT1767-3.3	●	19	27.5	39	kΩ
	LT1767-5	●	29	42	60	kΩ
Error Amp Voltage Gain	0.4V ≤ V_C ≤ 0.9V		150	350		
Error Amp Transconductance	ΔI_{VC} = ±10µA	●	500	850	1300	µMho
V_C Pin Source Current	V_{FB} = V_{NOM} – 17%	●	80	120	160	µA
V_C Pin Sink Current	V_{FB} = V_{NOM} + 17%	●	70	110	180	µA
V_C Pin to Switch Current Transconductance				2.5		A/V
V_C Pin Minimum Switching Threshold	Duty Cycle = 0%			0.35		V
V_C Pin 1.5A I_{SW} Threshold				0.9		V
Maximum Switch Duty Cycle	V_C = 1.2V, I_{SW} = 400mA		85	90		%
		●	80			%
Minimum Boost Voltage Above Switch	I_{SW} = –1.5A, 0°C ≤ T_A ≤ 125°C and –1.3A, T_A < 0°C	●		1.8	2.7	V
Boost Current	I_{SW} = –0.5A (Note 4)	●		10	15	mA
	I_{SW} = –1.5A, 0°C ≤ T_A ≤ 125°C and –1.3A, T_A < 0°C (Note 4)	●		30	45	mA
$\overline{SHDN}$ Threshold Voltage		●	1.27	1.33	1.40	V
$\overline{SHDN}$ Input Current (Shutting Down)	$\overline{SHDN}$ = 60mV Above Threshold	●	–7	–10	–13	µA
$\overline{SHDN}$ Threshold Current Hysteresis	$\overline{SHDN}$ = 100mV Below Threshold	●	4	7	10	µA
SYNC Threshold Voltage				1.5	2.2	V
SYNC Input Frequency			1.5		2	MHz
SYNC Pin Resistance	I_{SYNC} = 1mA			20		kΩ

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

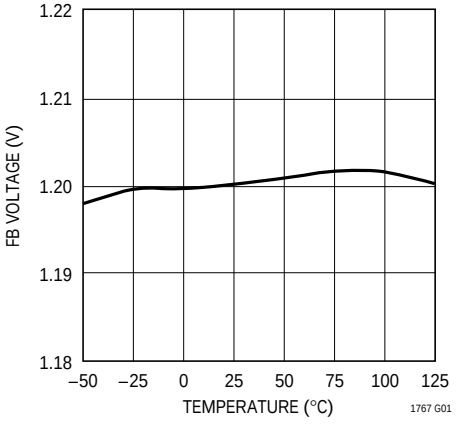
Note 2: The LT1767E is guaranteed to meet performance specifications from 0°C to 125°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Minimum input voltage is defined as the voltage where the internal regulator enters lockout. Actual minimum input voltage to maintain a regulated output will depend on output voltage and load current. See Applications Information.

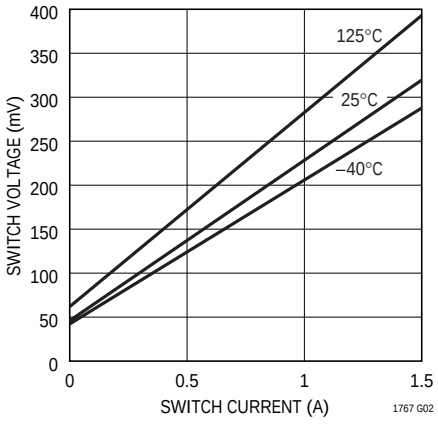
Note 4: Current flows into the BOOST pin only during the on period of the switch cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

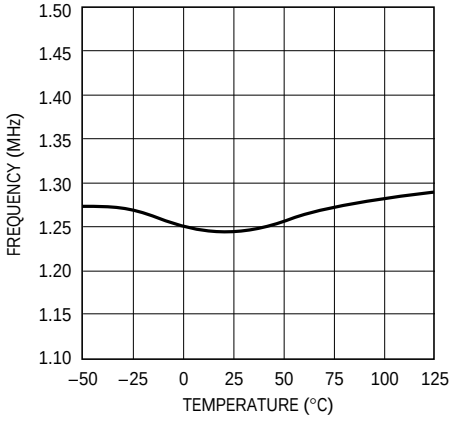
FB vs Temperature (Adj)



Switch On Voltage Drop

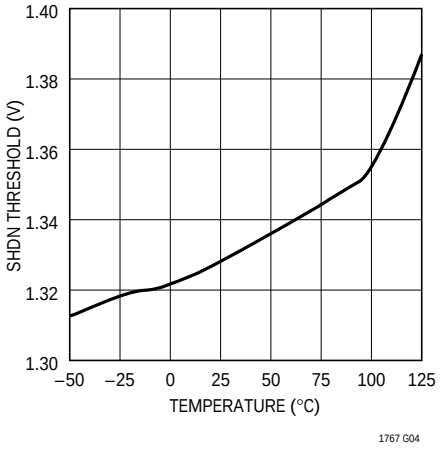


Oscillator Frequency

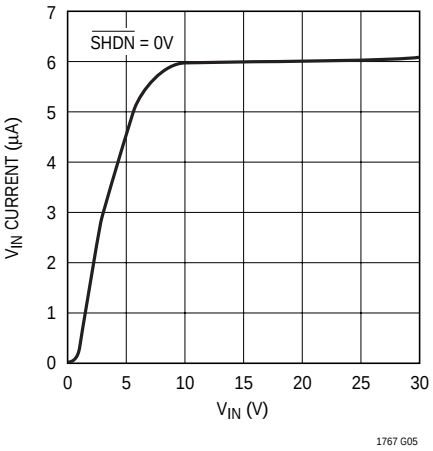


TYPICAL PERFORMANCE CHARACTERISTICS

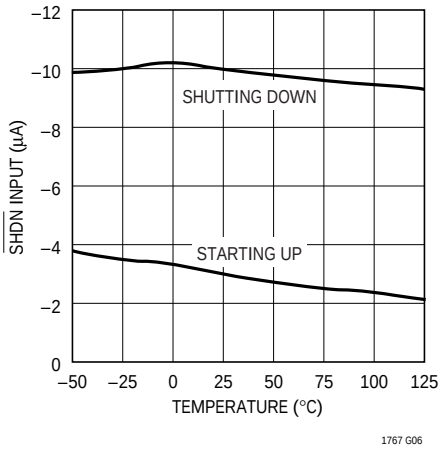
$\overline{SHDN}$ Threshold vs Temperature



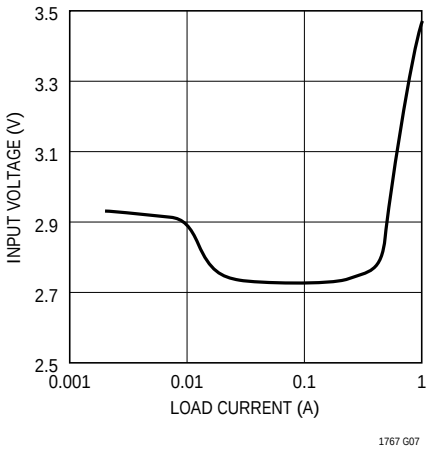
$\overline{SHDN}$ Supply Current vs V_{IN}



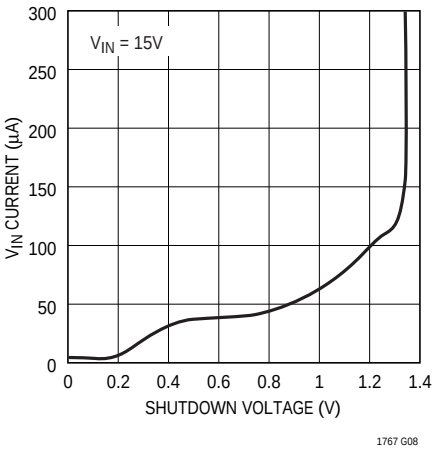
$\overline{SHDN}$ I_P Current vs Temperature



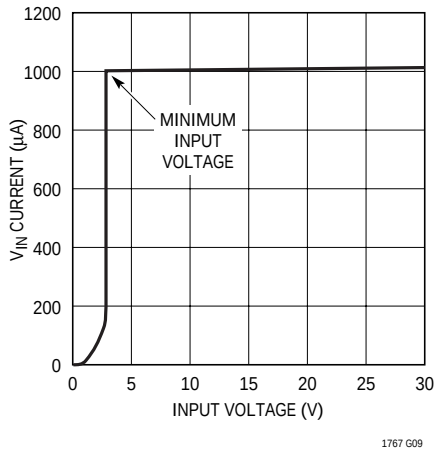
Minimum Input Voltage for 2.5V Out



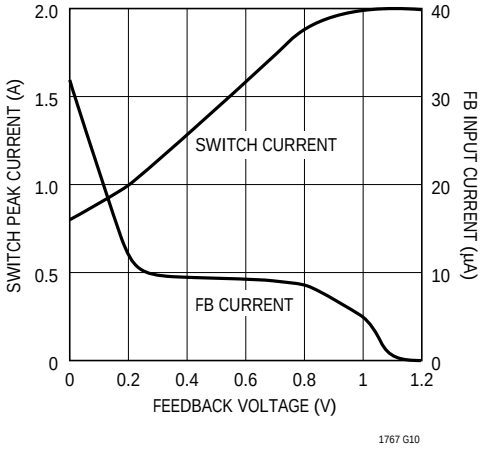
$\overline{SHDN}$ Supply Current



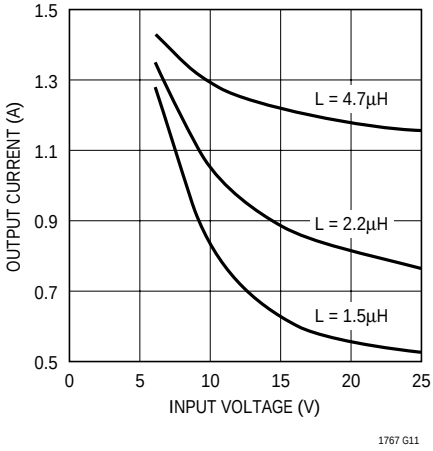
Input Supply Current



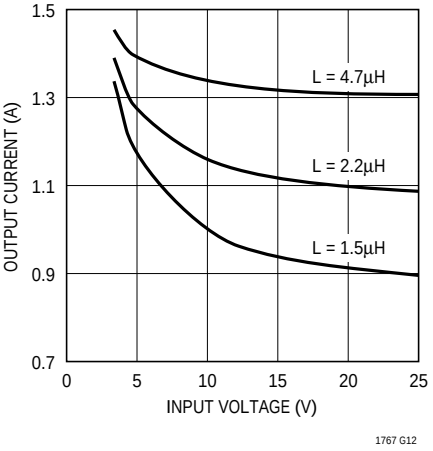
Current Limit Foldback



Maximum Load Current, V_{OUT} = 5V



Maximum Load Current, V_{OUT} = 2.5V



PIN FUNCTIONS

FB: The feedback pin is used to set output voltage using an external voltage divider that generates 1.2V at the pin with the desired output voltage. The fixed voltage 1.8V, 2.5V, 3.3V and 5V versions have the divider network included internally and the FB pin is connected directly to the output. If required, the current limit can be reduced during start up or short-circuit when the FB pin is below 0.5V (see the Current Limit Foldback graph in the Typical Performance Characteristics section). An impedance of less than 5kΩ (adjustable part only) at the FB pin is needed for this feature to operate.

BOOST: The BOOST pin is used to provide a drive voltage, higher than the input voltage, to the internal bipolar NPN power switch. Without this added voltage, the typical switch voltage loss would be about 1.5V. The additional boost voltage allows the switch to saturate and voltage loss approximates that of a 0.22Ω FET structure.

V_{IN}: This is the collector of the on-chip power NPN switch. This pin powers the internal circuitry and internal regulator. At NPN switch on and off, high dI/dt edges occur on this pin. Keep the external bypass capacitor and catch diode close to this pin. All trace inductance in this path will create a voltage spike at switch off, adding to the V_{CE} voltage across the internal NPN.

GND: The GND pin acts as the reference for the regulated output, so load regulation will suffer if the ÒgroundÓ end of the load is not at the same voltage as the GND pin of the IC. This condition will occur when load current or other currents flow through metal paths between the GND pin and the load ground point. Keep the ground path short between the GND pin and the load and use a ground plane when possible. Keep the path between the input bypass and the GND pin short. The GND pin of the MS8 package is directly attached to the internal tab. This pin should be attached to a large copper area to improve thermal resistance. The exposed pad of the MS8E package is also connected to GND. This should be soldered to a large copper area to improve its thermal resistance.

V_{SW}: The switch pin is the emitter of the on-chip power NPN switch. This pin is driven up to the input pin voltage during switch on time. Inductor current drives the switch pin negative during switch off time. Negative voltage must be clamped with an external catch diode with $V_{BR} \geq 0.8V$.

SYNC: The sync pin is used to synchronize the internal oscillator to an external signal. It is directly logic compatible and can be driven with any signal between 20% and 80% duty cycle. The synchronizing range is equal to *or above* the initial operating frequency, up to 2MHz. See Synchronization section in Applications Information for details. When not in use, this pin should be grounded.

$\overline{SHDN}$: The shutdown pin is used to turn off the regulator and to reduce input drain current to a few microamperes. The 1.33V threshold can function as an accurate undervoltage lockout (UVLO), preventing the regulator from operating until the input voltage has reached a predetermined level. Float or pull high to put the regulator in the operating mode.

V_C: The V_C pin is the output of the error amplifier and the input of the peak switch current comparator. It is normally used for frequency compensation, but can do double duty as a current clamp or control loop override. This pin sits at about 0.35V for very light loads and 0.9V at maximum load. It can be driven to ground to shut off the output.

BLOCK DIAGRAM

The LT1767 is a constant frequency, current mode buck converter. This means that there is an internal clock and two feedback loops that control the duty cycle of the power switch. In addition to the normal error amplifier, there is a current sense amplifier that monitors switch current on a cycle-by-cycle basis. A switch cycle starts with an oscillator pulse which sets the RS flip-flop to turn the switch on. When switch current reaches a level set by the inverting input of the comparator, the flip-flop is reset and the switch turns off. Output voltage control is obtained by using the output of the error amplifier to set the switch current trip point. This technique means that the error amplifier commands current to be delivered to the output rather than voltage. A voltage fed system will have low phase shift up to the resonant frequency of the inductor and output capacitor, then an abrupt 180° shift will occur. The current fed system will have 90° phase shift at a much lower frequency, but will not have the additional 90° shift until well beyond the LC resonant frequency. This makes it much easier to frequency compensate the feedback loop and also gives much quicker transient response.

High switch efficiency is attained by using the BOOST pin to provide a voltage to the switch driver which is higher than the input voltage, allowing switch to be saturated. This boosted voltage is generated with an external capacitor and diode. A comparator connected to the shutdown pin disables the internal regulator, reducing supply current.

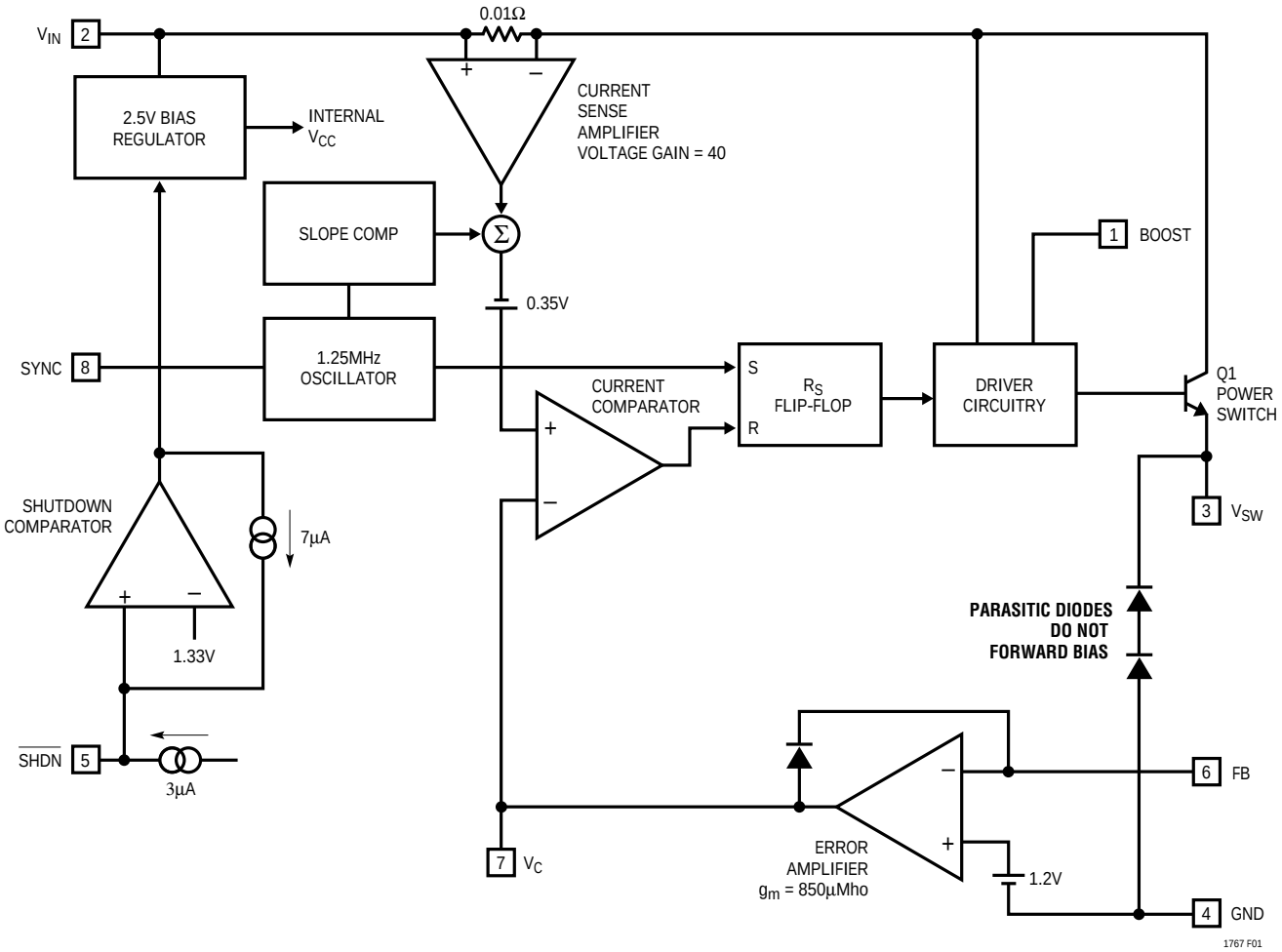


Figure 1. Block Diagram

APPLICATIONS INFORMATION

FB RESISTOR NETWORK

If an output voltage of 1.8V, 2.5V, 3.3V or 5V is required, the respective fixed option part, -1.8, -2.5, -3.3 or -5, should be used. The FB pin is tied directly to the output; the necessary resistive divider is already included on the part. For other voltage outputs, the adjustable part should be used and an external resistor divider added. The suggested resistor (R2) from FB to ground is 10k. This reduces the contribution of FB input bias current to output voltage to less than 0.25%. The formula for the resistor (R1) from V_{OUT} to FB is:

$$R1 = \frac{R2\left(V_{OUT} - 1.2\right)}{1.2 - R2(0.25\mu A)}$$

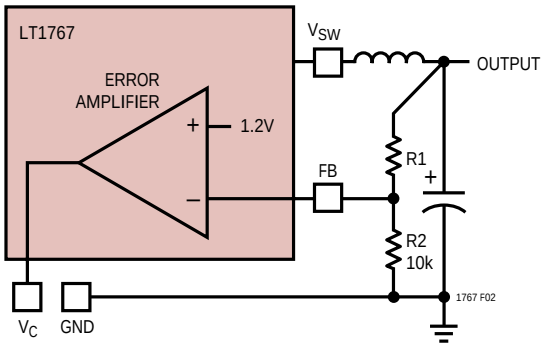


Figure 2. Feedback Network

INPUT CAPACITOR

Step-down regulators draw current from the input supply in pulses. The rise and fall times of these pulses are very fast. The input capacitor is required to reduce the voltage ripple this causes at the input of LT1767 and force the switching current into a tight local loop, thereby minimizing EMI. The RMS ripple current can be calculated from:

$$I_{RIPPLE(RMS)} = I_{OUT}\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right) / V_{IN}^2}$$

Higher value, lower cost ceramic capacitors are now available in smaller case sizes. These are ideal for input bypassing since their high frequency capacitive nature removes most ripple current rating and turn-on surge problems. At higher switching frequency, the energy storage requirement of the input capacitor is reduced so values in the range of 1µF to 4.7µF are suitable for most applications. X5R or similar type ceramics can be used since the absolute value of capacitance is less important and has no significant effect on loop stability. If operation is required close to the minimum input required by the output of the LT1767, a larger value may be required. This is to prevent excessive ripple causing dips below the minimum operating voltage, resulting in erratic operation.

If tantalum capacitors are used, values in the 22µF to 470µF range are generally needed to minimize ESR and meet ripple current and surge ratings. Care should be taken to ensure the ripple and surge ratings are not exceeded. The AVX TPS and Kemet T495 series are surge rated. AVX recommends derating capacitor operating voltage by 2:1 for high surge applications.

OUTPUT CAPACITOR

Unlike the input capacitor, RMS ripple current in the output capacitor is normally low enough that ripple current rating is not an issue. The current waveform is triangular, with an RMS value given by:

$$I_{RIPPLE(RMS)} = \frac{0.29\left(V_{OUT}\right)\left(V_{IN} - V_{OUT}\right)}{\left(L\right)\left(f\right)\left(V_{IN}\right)}$$

The LT1767 will operate with both ceramic and tantalum output capacitors. Ceramic capacitors are generally chosen for their small size, very low ESR (effective series resistance), and good high frequency operation, reducing output ripple voltage. Their low ESR removes a useful zero in the loop frequency response, common to tantalum capacitors. To compensate for this, the V_C loop compensation pole frequency must typically be reduced by a factor of 10. Typical ceramic output capacitors are in the 1µF to 10µF range. Since the absolute value of capacitance defines the pole frequency of the output stage, an X7R or X5R type ceramic, which have good temperature stability, is recommended.

Tantalum capacitors are usually chosen for their bulk capacitance properties, useful in high transient load applications. ESR rather than capacitive value defines output ripple at 1.25MHz. Typical LT1767 applications require a tantalum capacitor with less than 0.8Ω ESR at 22µF to 500µF, see Table 2.

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Table 2. Surface Mount Solid Tantalum Capacitor ESR and Ripple Current

E Case Size	ESR (Max, Ω)	Ripple Current (A)
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
AVX TAJ	0.7 to 0.9	0.4
D Case Size		
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
C Case Size		
AVX TPS	0.2 (typ)	0.5 (typ)

Figure 3 shows a comparison of output ripple for a ceramic and tantalum capacitor at 200mA ripple current.

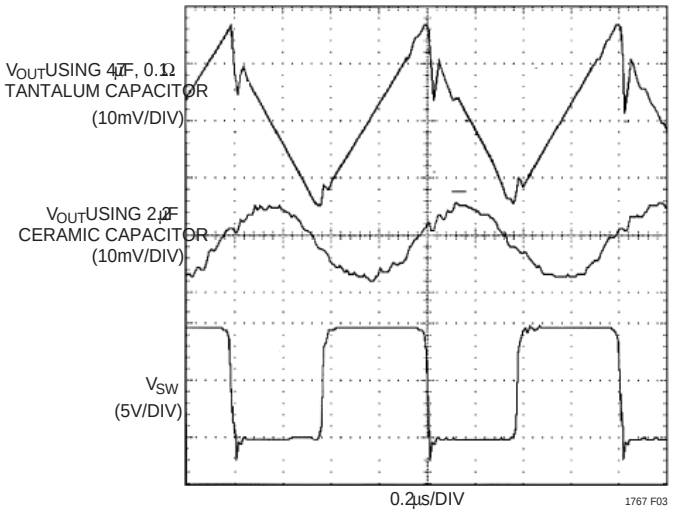

Figure 3. Output Ripple Voltage Waveform

INDUCTOR CHOICE AND MAXIMUM OUTPUT CURRENT

Maximum output current for a buck converter is equal to the maximum switch rating (I_P) minus one half peak to peak inductor current. In past designs, the maximum switch current has been reduced by the introduction of slope compensation. Slope compensation is required at duty cycles above 50% to prevent an affect called subharmonic oscillation (see Application Note 19 for details). The LT1767 has a new circuit technique that maintains a constant switch current rating at all duty cycles. (Patent Pending)

For most applications, the output inductor will be in the 1µH to 10µH range. Lower values are chosen to reduce the physical size of the inductor, higher values allow higher output currents due to reduced peak to peak ripple current, and reduces the current at which discontinuous operation occurs. The following formula gives maximum output current for continuous mode operation, implying that the peak to peak ripple (2x the term on the right) is less than the maximum switch current.

Continuous Mode

$$I_{OUT(MAX)} = I_P - \frac{(V_{OUT})(V_{IN} - V_{OUT})}{2(L)(f)(V_{IN})}$$

Discontinuous operation occurs when

$$I_{OUT(DIS)} = \frac{(V_{OUT})}{2(L)(f)}$$

For V_{IN} = 8V, V_{OUT} = 5V and L = 3µH,

$$I_{OUT(MAX)} = 1.5 - \frac{(5)(8-5)}{2(3.3 \bullet 10^{-6})(1.25 \bullet 10^{6})(8)}$$

$$= 1.5 - 0.23 = 1.27\,A$$

Note that the worst case (minimum output current available) condition is at the maximum input voltage. For the same circuit at 15V, maximum output current would be only 1.1A.

When choosing an inductor, consider maximum load current, core and copper losses, allowable component height, output voltage ripple, EMI, fault current in the inductor, saturation, and of course, cost. The following procedure is suggested as a way of handling these somewhat complicated and conflicting requirements.

1. Choose a value in microhenries from the graphs of maximum load current. Choosing a small inductor with lighter loads may result in discontinuous mode of operation, but the LT1767 is designed to work well in either mode.

Assume that the average inductor current is equal to load current and decide whether or not the inductor must withstand continuous fault conditions. If maximum load current is 0.5A, for instance, a 0.5A inductor may not survive a continuous 2A overload condition. Also, the instantaneous application of input or release from shutdown, at high input voltages, may cause

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saturation of the inductor. In these applications, the soft-start circuit shown in Figure 10 should be used.

2. Calculate peak inductor current at full load current to ensure that the inductor will not saturate. Peak current can be significantly higher than output current, especially with smaller inductors and lighter loads, so donÕt omit this step. Powdered iron cores are forgiving because they saturate softly, whereas ferrite cores saturate abruptly. Other core materials fall somewhere in between.

$$I_{PEAK} = I_{OUT} + \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{2\left(L\right)\left(f\right)\left(V_{IN}\right)}$$

V_{IN} = Maximum input voltage
f = Switching frequency, 1.25MHz

3. Decide if the design can tolerate an ÒopenÓ core geometry like a rod or barrel, which have high magnetic field radiation, or whether it needs a closed core like a toroid to prevent EMI problems. This is a tough decision because the rods or barrels are temptingly cheap and small and there are no helpful guidelines to calculate when the magnetic field radiation will be a problem.

Table 3

PART NUMBER	VALUE (uH)	I_{SAT}(Amps)	DCR (Ω)	HEIGHT (mm)
Coiltronics				
TP1-2R2	2.2	1.3	0.188	1.8
TP2-2R2	2.2	1.5	0.111	2.2
TP3-4R7	4.7	1.5	0.181	2.2
TP4- 100	10	1.5	0.146	3.0
Murata				
LQH1C1R0M04	1.0	0.51	0.28	1.8
LQH3C1R0M24	1.0	1.0	0.06	2.0
LQH3C2R2M24	2.2	0.79	0.1	2.0
LQH4C1R5M04	1.5	1.0	0.09	2.6
Sumida				
CD73- 100	10	1.44	0.080	3.5
CDRH4D18-2R2	2.2	1.32	0.058	1.8
CDRH5D18-6R2	6.2	1.4	0.071	1.8
CDRH5D28-100	10	1.3	0.048	2.8

4. After making an initial choice, consider the secondary things like output voltage ripple, second sourcing, etc. Use the experts in the Linear TechnologyÕs applications department if you feel uncertain about the final choice. They have experience with a wide range of inductor types and can tell you about the latest developments in low profile, surface mounting, etc.

CATCH DIODE

The suggested catch diode (D1) is a UPS120 Schottky, or its Motorola equivalent, MBRM120LTI/MBRM130LTI. It is rated at 2A average forward current and 20V/30V reverse voltage. Typical forward voltage is 0.5V at 1A. The diode conducts current only during switch off time. Peak reverse voltage is equal to regulator input voltage. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = \frac{I_{OUT}\left(V_{IN} - V_{OUT}\right)}{V_{IN}}$$

BOOST PIN

For most applications, the boost components are a 0.1µF capacitor and a CMDSH-3 diode. The anode is typically connected to the regulated output voltage to generate a voltage approximately V_{OUT} above V_{IN} to drive the output stage. The output driver requires at least 2.7V of headroom throughout the on period to keep the switch fully saturated. However, the output stage discharges the boost capacitor during the on time. If the output voltage is less than 3.3V, it is recommended that an alternate boost supply is used. The boost diode can be connected to the input, although, care must be taken to prevent the 2x V_{IN} boost voltage from exceeding the BOOST pin absolute maximum rating. The additional voltage across the switch driver also increases power loss, reducing efficiency. If available, an independent supply can be used with a local bypass capacitor.

A 0.1µF boost capacitor is recommended for most applications. Almost any type of film or ceramic capacitor is

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suitable, but the ESR should be <1Ω to ensure it can be fully recharged during the off time of the switch. The capacitor value is derived from worst-case conditions of 700ns on-time, 50mA boost current, and 0.7V discharge ripple. This value is then guard banded by 2x for secondary factors such as capacitor tolerance, ESR and temperature effects. The boost capacitor value could be reduced under less demanding conditions, but this will not improve circuit operation or efficiency. Under low input voltage and low load conditions, a higher value capacitor will reduce discharge ripple and improve start up operation.

SHUTDOWN AND UNDERVOLTAGE LOCKOUT

Figure 4 shows how to add undervoltage lockout (UVLO) to the LT1767. Typically, UVLO is used in situations where the input supply is *current limited* or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. UVLO prevents the regulator from operating at source voltages where these problems might occur.

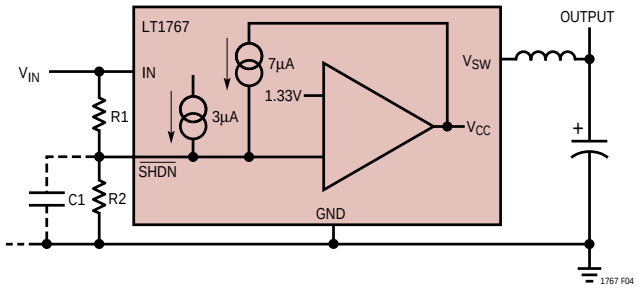

Figure 4. Undervoltage Lockout

An internal comparator will force the part into shutdown below the minimum V_{IN} of 2.6V. This feature can be used to prevent excessive discharge of battery-operated systems. If an adjustable UVLO threshold is required, the shutdown pin can be used. The threshold voltage of the shutdown pin comparator is 1.33V ±4%. An internal current source defaults the open pin condition to be operating (see Typical Performance Graphs). Current hysteresis is added above the SHDN threshold. This can be used to set voltage hysteresis of the UVLO using the following:

$$R1 = \frac{V_H - V_L}{7\mu A}$$

$$R2 = \frac{1.33V}{\frac{\left(V_H - 1.33V\right)}{R1} + 3\mu A}$$

V_H Đ Turn-on threshold

V_L Đ Turn-off threshold

Example: switching should not start until the input is above 4.75V and is to stop if the input falls below 3.75V.

$V_H = 4.75V$

$V_L = 3.75V$

$$R1 = \frac{4.75V - 3.75V}{7\mu A} = 143k$$

$$R2 = \frac{1.33V}{\frac{\left(4.75V - 1.33V\right)}{143k} + 3\mu A} = 49.4k$$

Keep the connections from the resistors to the SHDN pin short and make sure that the interplane or surface capacitance to the switching nodes are minimized. If high resistor values are used, the SHDN pin should be bypassed with a 1nF capacitor to prevent coupling problems from the switch node.

SYNCHRONIZATION

The SYNC pin, is used to synchronize the internal oscillator to an external signal. The SYNC input must pass from a logic level low, through the maximum synchronization threshold with a duty cycle between 20% and 80%. The input can be driven directly from a logic level output. The synchronizing range is equal to the *initial* operating frequency up to 2MHz. This means that the *minimum* practical sync frequency is equal to the worst-case *high* self-oscillating frequency (1.5MHz), not the typical operating frequency of 1.25MHz. Caution should be used when synchronizing above 1.6MHz because at higher sync frequencies the amplitude of the internal slope compensation used to

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prevent subharmonic switching is reduced. This type of subharmonic switching only occurs at input voltages less than twice output voltage. Higher inductor values will tend to eliminate this problem. See Frequency Compensation section for a discussion of an entirely different cause of subharmonic switching before assuming that the cause is insufficient slope compensation. Application Note 19 has more details on the theory of slope compensation.

LAYOUT CONSIDERATIONS

As with all high frequency switchers, when considering layout, care must be taken in order to achieve optimal electrical, thermal and noise performance. For maximum efficiency, switch rise and fall times are typically in the nanosecond range. To prevent noise both radiated and conducted, the high speed switching current path, shown in Figure 5, must be kept as short as possible. This is implemented in the suggested layout of Figure 6. Shortening this path will also reduce the parasitic trace inductance of approximately 25nH/inch. At switch off, this parasitic inductance produces a flyback spike across the LT1767 switch. When operating at higher currents and input voltages, with poor layout, this spike can generate voltages across the LT1767 that may exceed its absolute maximum rating. A ground plane should always be used under the switcher circuitry to prevent interplane coupling and overall noise.

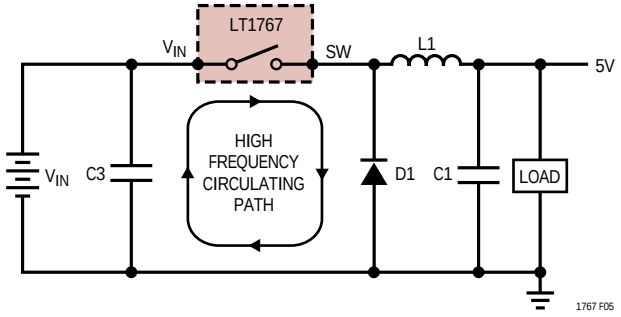

Figure 5. High Speed Switching Path

The V_C and FB components should be kept as far away as possible from the switch and boost nodes. The LT1767 pinout has been designed to aid in this. The ground for these components should be separated from the switch current path. Failure to do so will result in poor stability or subharmonic like oscillation.

Board layout also has a significant effect on thermal resistance. Soldering the exposed pad to as large a copper area as possible and placing feedthroughs under the pad to a ground plane, will reduce die temperature and increase the power capacity of the LT1767. For the exposed package, Pin 4 is connected directly to the pad inside the package. Similar treatment of this pin will result in lower die temperatures.

THERMAL CALCULATIONS

Power dissipation in the LT1767 chip comes from four sources: switch DC loss, switch AC loss, boost circuit current, and input quiescent current. The following formulas show how to calculate each of these losses. These formulas assume continuous mode operation, so they should not be used for calculating efficiency at light load currents.

Switch loss:

$$P_{SW} = \frac{R_{SW}\left(I_{OUT}\right)^2\left(V_{OUT}\right)}{V_{IN}} + 17ns\left(I_{OUT}\right)\left(V_{IN}\right)\left(f\right)$$

Boost current loss for $V_{BOOST} = V_{OUT}$:

$$P_{BOOST} = \frac{V_{OUT}^2\left(I_{OUT}/50\right)}{V_{IN}}$$

Quiescent current loss:

$$P_Q = V_{IN}\left(0.001\right)$$

R_{SW} = Switch resistance (0.27Ω when hot)
17ns = Equivalent switch current/voltage overlap time
f = Switch frequency
Example: with V_{IN} = 10V, V_{OUT} = 5V and I_{OUT} = 1A:

$$P_{SW} = \frac{\left(0.27\right)\left(1\right)^2\left(5\right)}{10} + \left(17 \bullet 10^{-9}\right)\left(1\right)\left(10\right)\left(1.25 \bullet 10^6\right)$$
$$= 0.135 + 0.21 = 0.34W$$

$$P_{BOOST} = \frac{\left(5\right)^2\left(1/50\right)}{10} = 0.05W$$

$$P_Q = 10\left(0.001\right) = 0.01W$$

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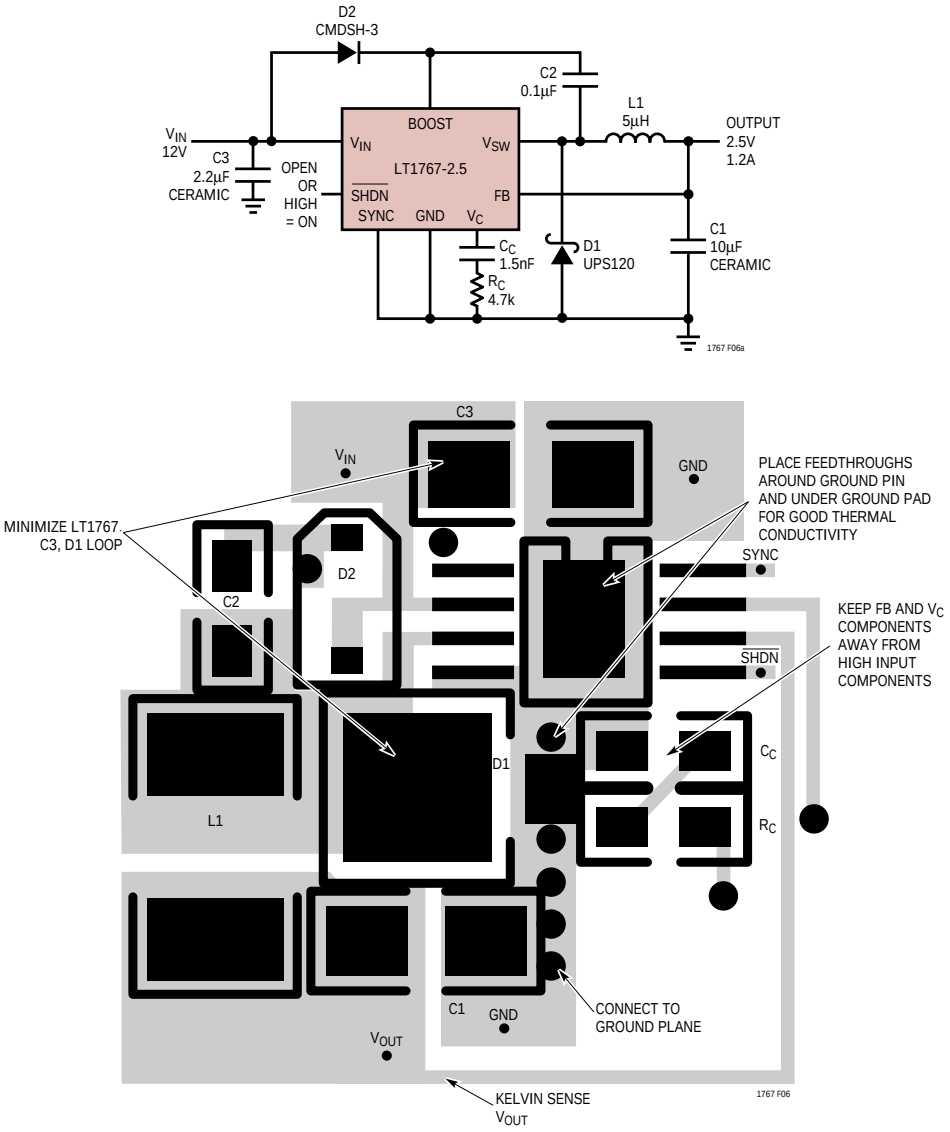

Figure 6. Typical Application and Suggested Layout (Topside Only Shown)

Total power dissipation is 0.34 + 0.05 + 0.01 = 0.4W. When estimating ambient, remember the nearby catch diode and inductor will also be dissipating power.

Thermal resistance for LT1767 package is influenced by the presence of internal or backside planes. With a full plane under the package, thermal resistance for the exposed pad package will be about 40°C/W. No plane will increase resistance to about 150°C/W. To calculate die temperature, use the appropriate thermal resistance number and add in worst-case ambient temperature:

$$T_J = T_A + \theta_{JA}(P_{TOT})$$

$$P_{DIODE} = \frac{(V_F)(V_{IN} - V_{OUT})(I_{LOAD})}{V_{IN}}$$

V_F = Forward voltage of diode (assume 0.5V at 1A)

$$P_{DIODE} = \frac{(0.5)(12-5)(1)}{12} = 0.29W$$

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Notice that the catch diodeÕs forward voltage contributes a significant loss in the overall system efficiency. A larger lower V_F diode can improve efficiency by several percent.

$P_{INDUCTOR} = (I_{LOAD})(L_{DCR})$

L_{DCR} = Inductor DC resistance (assume 0.1Ω)

$P_{INDUCTOR} = (1)(0.1) = 0.1W$

Typical thermal resistance of the board is 35°C/W. At an ambient temperature of 65°C,

$T_j = 65 + 40(0.4) + 35(0.39) = 95°C$

If a true die temperature is required, a measurement of the SYNC to GND pin resistance can be used. The SYNC pin resistance across temperature must first be calibrated, with no device power, in an oven. The same measurement can then be used in operation to indicate the die temperature.

FREQUENCY COMPENSATION

Before starting on the theoretical analysis of frequency response, the following should be remembered Ð the worse the board layout, the more difficult the circuit will be to stabilize. This is true of almost all high frequency analog circuits, read the ÔLAYOUT CONSIDERATIONSÕ section first. Common layout errors that appear as stability problems are distant placement of input decoupling capacitor and/or catch diode, and connecting the V_C compensation to a ground track carrying significant switch current. In addition, the theoretical analysis considers only first order non-ideal component behavior. For these reasons, it is important that a final stability check is made with production layout and components.

The LT1767 uses current mode control. This alleviates many of the phase shift problems associated with the inductor. The basic regulator loop is shown in Figure 7, with both tantalum and ceramic capacitor equivalent circuits. The LT1767 can be considered as two blocks, the error amplifier and the power stage.

Figure 8 shows the overall loop response with a 330pF V_C capacitor and a typical 100µF tantalum output capacitor. The response is set by the following terms:

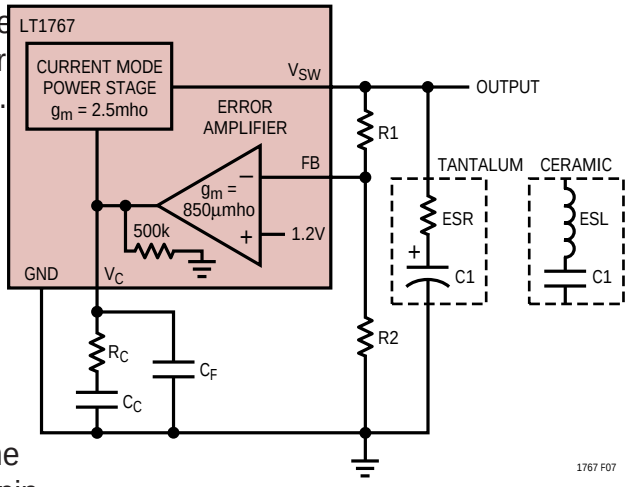

Figure 7. Model for Loop Response

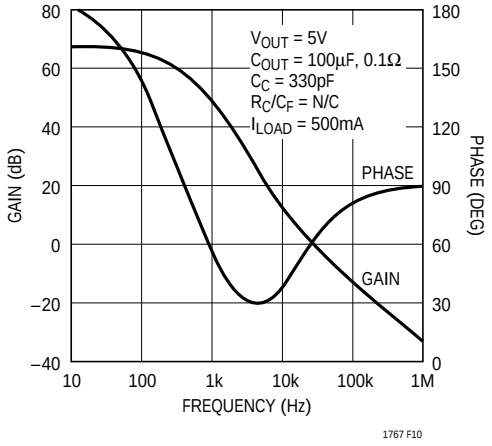

Figure 8. Overall Loop Response

Error amplifier:

DC gain set by g_m and R_L = 850µ ¥ 500kÊ =Ê 425.

Pole set by C_C and R_L = $(2\pi \text{ ¥ } 500k \text{ ¥ } 330p)^{-1}$ = 965Hz.

Unity-gain set by C_C and g_m = $(2\pi \text{ ¥ } 330p \text{ ¥ } 850\mu)^{-1}$ = 410kHz.

Power stage:

DC gain set by g_m and R_L (assume 1Ω) = 2.5 ¥ 10 = 25.

Pole set by C_{OUT} and R_L = $(2\pi \text{ ¥ } 100\mu \text{ ¥ } 10)^{-1}$ = 159Hz.

Unity-gain set by C_{OUT} and g_m = $(2\pi \text{ ¥ } 100\mu \text{ ¥ } 2.5)^{-1}$ = 3.98kHz.

Tantalum output capacitor:

Zero set by C_{OUT} and C_{ESR} = $(2\pi \text{ ¥ } 100\mu \text{ ¥ } 0.1)^{-1}$ = 15.9kHz.

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The zero produced by the ESR of the tantalum output capacitor is very useful in maintaining stability. Ceramic output capacitors do not have a zero due to very low ESR, but are dominated by their ESL. They form a notch in the 1MHz to 10MHz range. Without this zero, the V$_C$ pole must be made dominant. A typical value of 2.2nF will achieve this.

If better transient response is required, a zero can be added to the loop using a resistor (R$_C$) in series with the compensation capacitor. As the value of R$_C$ is increased, transient response will generally improve, but two effects limit its value. First, the combination of output capacitor ESR and a large R$_C$ may stop loop gain rolling off altogether. Second, if the loop gain is not rolled sufficiently at the switching frequency, output ripple will perturb the V$_C$ pin enough to cause unstable duty cycle switching similar to subharmonic oscillation. This may not be apparent at the output. Small signal analysis will not show this since a continuous time system is assumed. If needed, an additional capacitor (C$_F$) can be added to form a pole at typically one fifth the switching frequency (If R$_C$ = ~ 5k, C$_F$ = ~ 100pF).

When checking loop stability, the circuit should be operated over the applicationÕs full voltage, current and temperature range. Any transient loads should be applied and the output voltage monitored for a well-damped behavior. See Application Note 76 for more details.

CONVERTER WITH BACKUP OUTPUT REGULATOR

In systems with a primary and backup supply, for example, a battery powered device with a wall adapter input, the output of the LT1767 can be held up by the backup supply with its input disconnected. In this condition, the SW pin will source current into the V$_{IN}$ pin. If the $\overline{SHDN}$ pin is held at ground, only the shut down current of 6µA will be pulled via the SW pin from the second supply. With the $\overline{SHDN}$ pin floating, the LT1767 will consume its quiescent operating current of 1mA. The V$_{IN}$ pin will also source current to any other components connected to the input line. If this load is greater than 10mA or the input could be shorted to ground, a series Schottky diode must be added, as shown in Figure 9. With these safeguards, the output can be held at voltages up to the V$_{IN}$ absolute maximum rating.

BUCK CONVERTER WITH ADJUSTABLE SOFT-START

Large capacitive loads or high input voltages can cause high input currents at start-up. Figure 10 shows a circuit that limits the dv/dt of the output at start-up, controlling the capacitor charge rate. The buck converter is a typical configuration with the addition of R3, R4, C$_{SS}$ and Q1. As the output starts to rise, Q1 turns on, regulating switch current via the V$_C$ pin to maintain a constant dv/dt at the output. Output rise time is controlled by the current through C$_{SS}$ defined by R4 and Q1Õs V$_{BE}$. Once the output is in regulation, Q1 turns off and the circuit operates normally. R3 is transient protection for the base of Q1.

$$RiseTime = \frac{(R4)(C_{SS})(V_{OUT})}{(V_{BE})}$$

Using the values shown in Figure 10,

$$RiseTime = \frac{(47 \bullet 10^{3})(15 \bullet 10^{-9})(5)}{0.7} = 5ms$$

The ramp is linear and rise times in the order of 100ms are possible. Since the circuit is voltage controlled, the ramp rate is unaffected by load characteristics and maximum output current is unchanged. Variants of this circuit can be used for sequencing multiple regulator outputs.

Dual Output SEPIC Converter

The circuit in Figure 11 generates both positive and negative 5V outputs with a single piece of magnetics. The two inductors shown are actually just two windings on a standard B H Electronics inductor. The topology for the 5V output is a standard buck converter. The Ð5V topology would be a simple flyback winding coupled to the buck converter if C4 were not present. C4 creates a SEPIC (single-ended primary inductance converter) topology which improves regulation and reduces ripple current in the L1. Without C4, the voltage swing on L1B compared to L1A would vary due to relative loading and coupling losses. C4 provides a low impedance path to maintain an equal voltage swing in L1B, improving regulation. In a flyback converter, during switch on time, all the converterÕs energy is stored in L1A only, since no current flows in L1B. At switch off, energy is transferred by magnetic coupling into L1B, powering the Ð5V rail. C4 pulls L1B positive

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during switch on time, causing current to flow, and energy to build in L1B and C4. At switch off, the energy stored in both L1B and C4 supply the ÐV rail. This reduces the current in L1A and changes L1B current waveform from square to triangular. For details on this circuit, including maximum output currents, see Design Note 100.

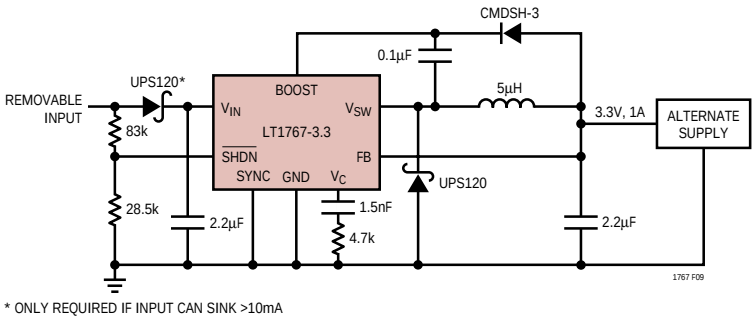


Figure 9. Dual Source Supply with 6µA Reverse Leakage

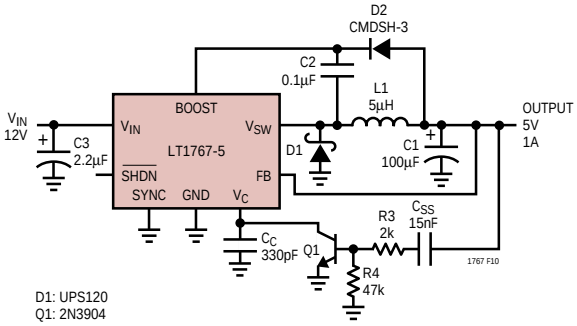


Figure 10. Buck Converter with Adjustable Soft-Start

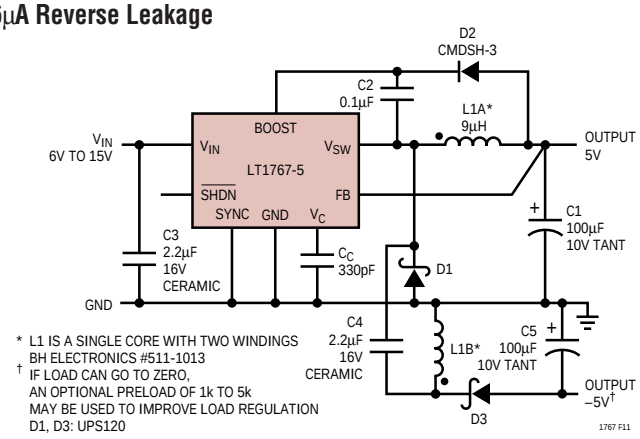
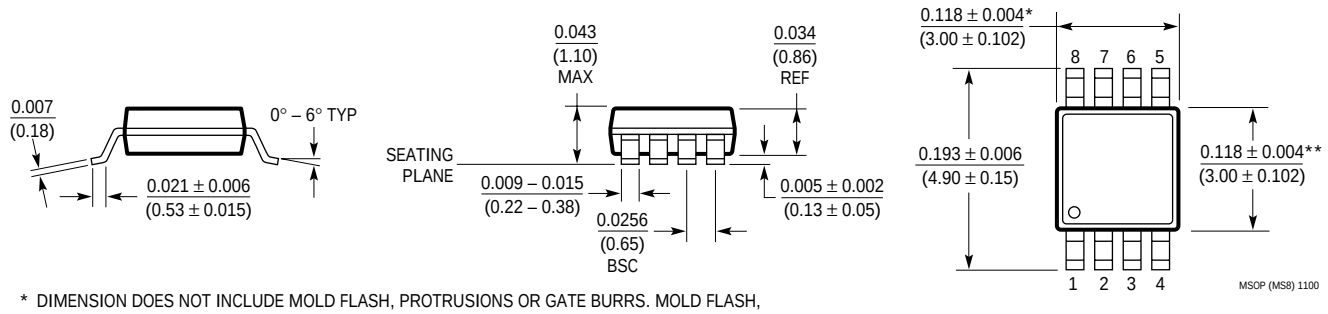


Figure 11. Dual Output SEPIC Converter

PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)

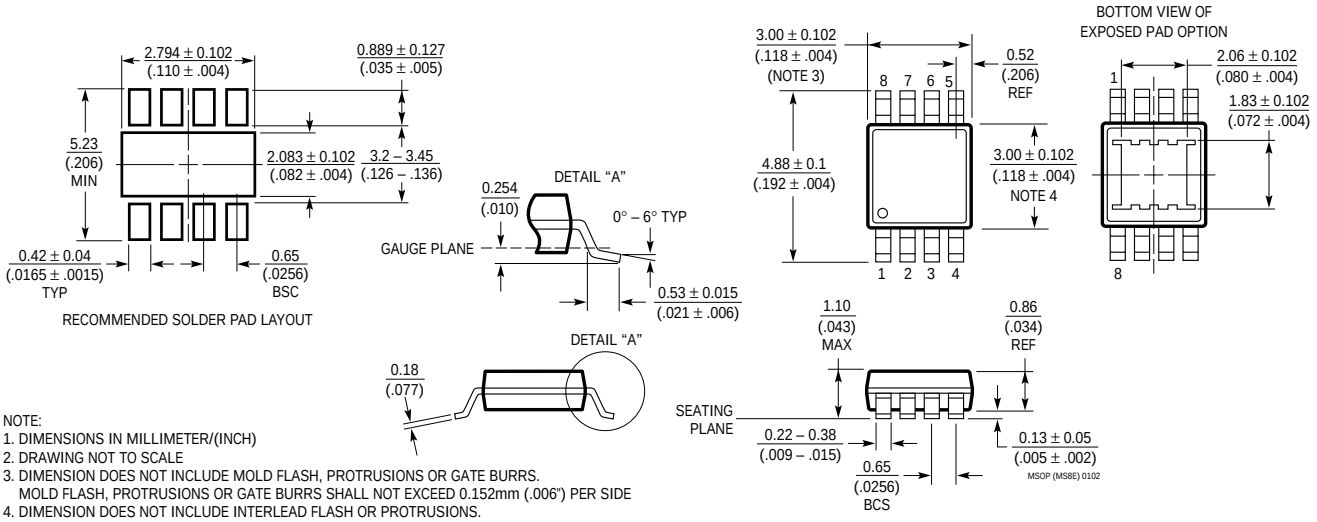


* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

PACKAGE DESCRIPTION

MS8E Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1662)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1370	High Efficiency DC/DC Converter	42V, 6A, 500kHz Switch
LT1371	High Efficiency DC/DC Converter	35V, 3A, 500kHz Switch
LT1372/LT1377	500kHz and 1MHz High Efficiency 1.5A Switching Regulators	Boost Topology
LT1374	High Efficiency Step-Down Switching Regulator	25V, 4.5A, 500kHz Switch
LT1375/LT1376	1.5A Step-Down Switching Regulators	500kHz, Synchronizable in SO-8 Package
LT1507	1.5A Step-Down Switching Regulator	500kHz, 4V to 16V Input, SO-8 Package
LT1576	1.5A Step-Down Switching Regulator	200kHz, Reduced EMI Generation
LT1578	1.5A Step-Down Switching Regulator	200kHz, Reduced EMI Generation
LT1616	600mA Step-Down Switching Regulator	1.4MHz, 4V to 25V Input, SOT-23 Package
LT1676/LT1776	Wide Input Range Step-Down Switching Regulators	60V Input, 700mA Internal Switches
LTC1765	1.25MHz, 3A Wide Input Range Step-Down DC/DC	T_H = 3W to 25V, SO-8 and TSSOP-16E Packages
LTC1877	High Efficiency Monolithic Step-Down Regulator	550kHz, MS8, V_{IN} to 10V, I_Q = 10µA, I_{OUT} to 600mA at V_{IN} = 5V
LTC1878	High Efficiency Monolithic Step-Down Regulator	550kHz, MS8, V_{IN} to 6V, I_Q = 10µA, I_{OUT} to 600mA at V_{IN} = 3.3V
LTC3401	Single Cell, High Current (1A), Micropower, Synchronous Step-Up DC/DC Converter	3MHz, V_{IN} = 0.5V to 5V, Up to 97% Efficiency Synchronizable Oscillator from 100kHz to 3MHz
LTC3402	Single Cell, High Current (2A), Micropower, Synchronous Step-Up DC/DC Converter	3MHz, V_{IN} = 0.7V to 5V, Up to 95% Efficiency Synchronizable Oscillator from 100kHz to 3MHz
LTC3404	1.4MHz High Efficiency, Monolithic Synchronous Step-Down Regulator	Up to 95% Efficiency, 100% Duty Cycle, IQ = 10µA, V_{IN} = 2.65V to 6V

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